# Data Acquisition for Multi-Channel CST of Aero-Engine Exhaust Plume Species and Combustion Diagnostics

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## ABSTRACT:

We present a tomographic system tailored to the measurement and study of aero-engine plume dynamics, exhaust chemistry and novel engine or fuel design. This aims to address aviation pollutant emission reductions. As the testing environment is not ideal for instrumentation and must not interfere with the operation or air flow of the engine, this data acquisition (DAQ) system utilises tunable-diode laser absorption spectroscopy (TDLAS) with wavelength modulation. Dithering increases SNR despite plume scintillation, but prompts exploration of accurate, at detector, real-time, digital lock-in (DLI) techniques. The readout options are restricted, forcing a custom, distributed architecture, embedded microprocessor control and Ethernet connectivity.

The multi-channel chemical species tomography (CST) electronics performs simultaneous detection and is scalable for increased numbers of beams, sample rates and laser dither rates. The system uses 12 digitisation hubs around the imaging space, each with 16 parallel channels. These operate at 40MS/s, 14bit, giving a system capacity of 192 channels and input rates exceeding 107Gbit/s. To meet the future needs of spectroscopy, gas species or beam extensions, the diagnostic tool allows software control over many signal processing and acquisition parameters.

This paper presents the design of the DAQ system through the entire custom electrical signal chain. Results are presented for a data interleaving approach aimed at reducing the impact of network packet loss when using UDP Ethernet protocols and high network utilisation. We also present gain and bandwidth results for all 192 analogue front-end circuits on the DAQ hubs, along with preliminary results for the optical detector and pre-amplifier circuits.

**Keywords**: Aero-Engines, Data Acquisition, Diagnostics, Digital-Lock-In, Gas-Tomography

## 1 INTRODUCTION:

To enable environmentally friendly aviation, while coping with increased global travel, the aviation industry requires the reduction of pollutant gas emissions. At the same time, increased fuel burning efficiency is of interest. While research into alternative fuels is ongoing, development is also investigating novel engines. To meet these demands, not only are understanding of combustion and engine operation needed, non-intrusive, high-speed measurement and imaging is required of multiple jet-engine exhaust plume gas species in both the spatial and temporal domains. Chemical Species Tomography (CST) instrumentation has been used in a similar manner, albeit on automotive engines (Wright et al, 2010). Those systems have predominantly used fixed-wavelengths, however by sweeping the wavelength, Tunable Diode Laser Absorption Spectroscopy (TDLAS), offers an established, robust technique for measuring gas parameters (Bain et al, 2013; Wilson et al, 2014).

TDLAS, which scans the optical wavelength, has been shown to be suitable for scalable multi-channel industrial diagnostic CST systems (Wilson et al, 2014); however other approaches using multi-mode absorption spectroscopy (Hamilton et al, 2010) may also be applicable. Wavelength Modulation

Spectroscopy (WMS) is often used, superimposed on the wavelength scan, to increase sensitivity. For gas detection in harsh environments and at low concentration, this works to our advantage, as the continued development of laser technologies can be combined with advances in Field Programmable Gate Arrays (FPGAs). For tomography, this allows efficient, low-noise, compact, high-speed and low-cost recovery of multi-beam absorption data (Chighine et al, 2015). With TDLAS being a highly selective spectroscopic technique, the absorption fingerprints of $CO_2$, $H_2O$, NOx or Unburnt-Hydrocarbons (UHC) can be detected. In comparison to single wavelength techniques, this allows properties such as concentration, pressure, and temperature to be obtained (Bain et al, 2013; Wilson et al 2014). Previous studies of TDLAS for jet engines, have shown the technique to i) be well suited to sharp absorption features, ii) have reduced calibration overheads and iii) increase measurement SNR in the presence of laser, plume or electronic noise (Wilson et al, 2014).

To extend the previous work on jet engine gas sensing (Harley et al, 2012; Sappey et al 2009) towards multi-beam tomography (Ma et al, 2013), a number of issues need to be resolved. A primary concern in optical beam array design is the practical development of a robust mechanical structure, this has been covered extensively in (Wright et al, 2016).

A significant issue with experimentation within an industrial testing setting, is the prohibitive distances between optical receiving electronics, the data acquisition (DAQ) system and the human user, in this case upwards of 50m. To avoid significant signal attenuation, additive noise and the costs of cabling, a distributed, hierarchical, primarily digital approach is taken. Further, as the testing environment is not ideal for high-cost, bulky instrumentation and must not interfere with the operation of the jet engine or the dynamics of the entrained air within the test cell, the presented DAQ is small, low-cost and is distributed around the imagine space.

The required outputs of this system for tomography are per-beam Path Concentration Integrals (PCIs). As such, the presented DAQ moves some of the required TDLAS/WMS demodulation and digital signal processing (DSP) onto the mechanical structure, where it can be performed in real-time and crucially provides an inherent data decimation important for reducing the significant data volumes. The distributed 12-node DAQ demodulates the TDLAS/WMS signal using FPGA-based Digital Lock-In Amplifier (DLIA) methods (Sappey et al 2009; Chighine et al, 2015), which can be significantly smaller and cheaper than the usual rack-mounted solutions (Lascos et al, 2008).

This paper puts forward the design and initial testing of a scalable, configurable DAQ for an exhaust plume diagnostic tomography system. To ensure the system is capable of operating as a scientific instrument, many system parameters are designed to be computer controlled. This includes control of the TDLAS/WMS laser modulation, the frequency and phase of the local DDS reference, the time constant of the DLIA and number of tomographic frames per second.



## 2 TOMOGRAPHIC SYSTEM DESIGN:

### 2.1 A Jet-Engine Diagnostics Chemical Species Tomography System

The mechanical structure used to obtain a robust co-planar imaging plane not only influences the available geometries of beams, but also influences the design of the DAQ system. The 7m diameter ‘ring’, ~4m aft of the aero-engine is discussed in detail within Wright et al, 2016. It uses 6 projections of 21 beams (126 beams in total) with concentrated beam crossings in the centre for a 1.4m exhaust plume diameter. The ring is a dodecagon (12-sided) to reduce mechanical engineering complexity and costs, while custom optical bread board mountings are used to ensure accurate positioning of the beam array (Figure 1). The ring is large as a) it must not affect the engine's entrainment air and b) the test cell detuner (thrust energy dissipater) must move into position freely. As the ring circumference is ~22m, and the nearest user-accessible computer is some 40-50m away (total worst case of ~70m), a per-beam cable architecture to a central data acquisition unit was discounted on cost, noise and receiving photodiode (PD) drive strength considerations. It is clear that as the number of beams increases, this approach would not be scalable, would incur significant cost and would yield poor measurement SNR. Likewise, the cost of rack-mount LIAs would force a time multiplexed DAQ structure, again difficult to scale for more beams and unsuitable for high gas speeds.

### 2.2 A Scalable Tomography System: Overview

To ensure low-noise, low-cost signalling, a distributed hierarchical architecture is used (Wright et al, 2016; Chighine et al, 2015). Firstly, this places trans-impedance amplification (TIA) and voltage pre-amplification next to each of the $CO_2$ dedicated InGaAs PDs. Secondly, each side of the dodecagon is

serviced by a local digitisation 'Hub' allowing pre-amplifier signals to be routed through only worst case ~2.5m of cable (Figure 1). This Hub digitises the signals of up to 16 channels, thus scalability can be obtained by increasing the number of utilised channels per Hub, increasing the number of Hubs on the ring and employing more pre-amplifiers. Each Hub utilises Ethernet connectivity with standard unique addressing, allowing the data readout to be fully scalable. As an example 24, 36, or 48 Hubs could be accommodated with ease. The current 12 Hub system has capacity for 192 fully simultaneous channels, with 126 channels dedicated to $CO_2$ tomographic measurement. This leaves 66 channels available for a) other gas species (e.g. UHC), b) extension of the $CO_2$ system beam count or c) spare channels for optical power monitoring or channel redundancy.

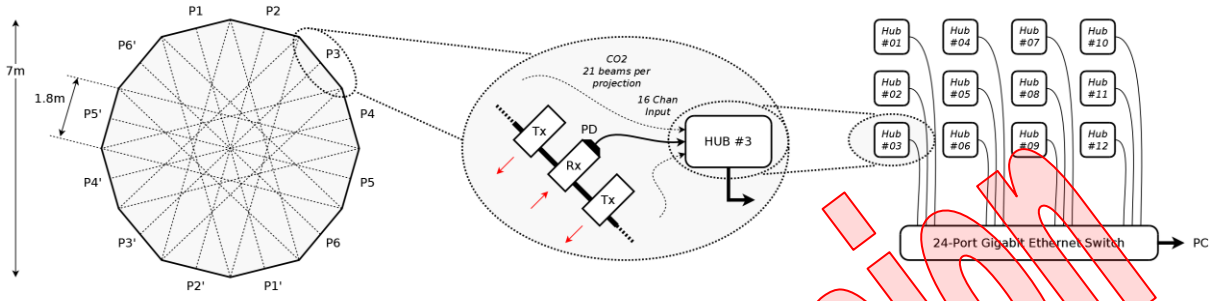


**Figure 1. CST System Overview: (Left) Mounting Ring, Beam Array and (Mid and Right) Distributed Data Acquisition.**



# 3 DATA ACQUISITION HARDWARE DESIGN:

## 3.1 Photodiodes and Pre-Amplifiers

Each receiving InGaAs photodiode uses a pre-amplifier (Figure 2), placed within the optical mounting. A differential TIA structure is used with a fixed gain of 100K Ohm, and is suitably compensated for the diode capacitance. The differential signals are then buffered through two high-current delivery op-amps for driving ~3m of ribbon cable. A 3MHz single-pole low-pass is introduced at the TIA a) ensuring gain flatness for up to a 500kHz laser dither frequency and a 1MHz maximum 2nd harmonic, b) allowing only signals of interest to be transmitted and c) starting frequency roll off to distribute the required anti-aliasing filter. Grounding requires special attention due to the prospect of multiple ground loops, therefore power and ground connections are made only at the Hubs.

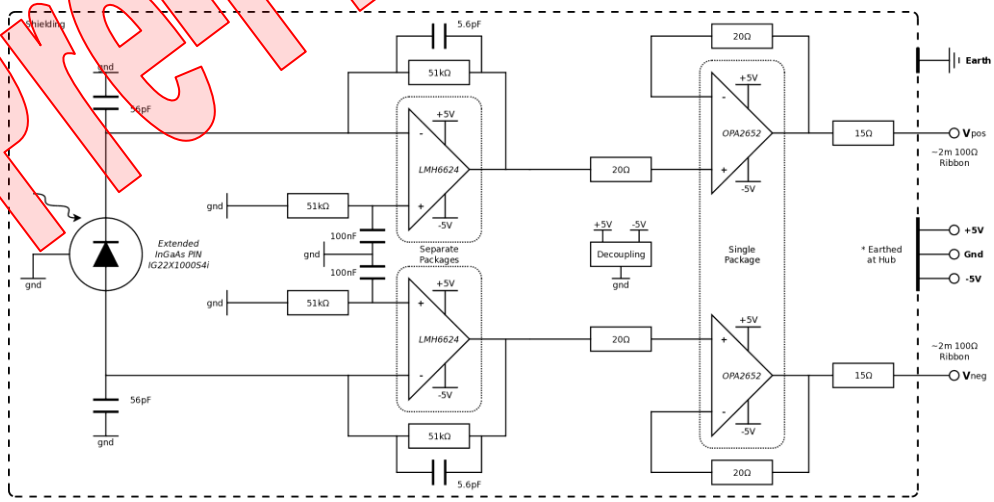


**Figure 2. 3MHz Low-Pass 100kOhm Differential TIA with Unity-Gain Line Driving Buffers.**

## 3.2 Hub Analogue/Digital Front-End

Each Hub incorporates both a 1st order 10Hz high-pass and 2nd order 3MHz low-pass filter. The latter is used along with the pre-amplifier pole to form the ADC anti-aliasing filter. The high-pass filter is used to cut the DC optical signal component. This is necessary to ensure that the laser power can be set to

utilise the majority of the ADC 2Vpp dynamic range without needing to accommodate potentially large changes in DC levels. While a narrow band-pass structure would be most suitable for lock-in amplification at a specific WMS frequency, it was decided to pass the dv/dt of the TDLAS amplitude ramp for system diagnostic and calibration reasons. The analogue signal is then digitised at 14bit resolution using a 40MS/s ADC (Figure 3). The sampling rate used is configurable, but gives some processing gain when considering the DSP and averaging utilised downstream.
The ADCs pass Low-Voltage Differential Signalling (LVDS) data in a serial (SerDes) Dual Data Rate (DDR) format to a central FPGA. This however must deal with incoming data rates in excess of 8.9Gb/s (560Mb/s per channel). This is a significant data overhead – a total of 107.5Gb/s – as such, methods of local demodulation must be utilised.

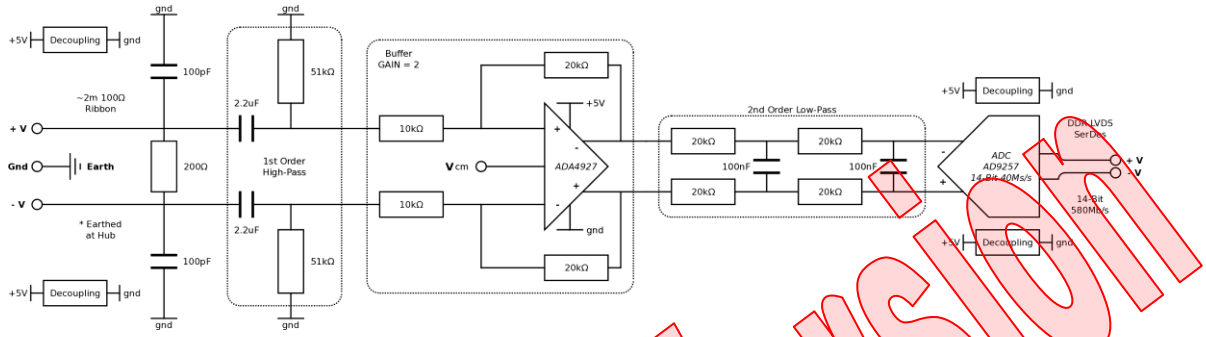


**Figure 3. The Analogue Front-End of a Single Channel, showing 3MHz 2nd Order Low-Pass, Buffering and 1st Order 10Hz High-Pass Filtering, prior to the 40MS/s 14bit Differential ADC.**

## 3.3 Hub Clocking Strategy

The octal packages for the ADCs allows simple high-speed clock routing for sampling. In this case, a central on-PCB Phase Locked Loop (PLL), provides two LVDS clocks for the two octal ADC packages, along with a low-noise system clock for the FPGA and embedded microprocessor (Figure 4). The design allows a symmetrical PCB layout, ensuring sampling time matching, while low-jitter ensures a low sampling phase-noise. The two ADC clocks can be phase and frequency shifted to reduce timing mismatch or to tailor the sampling rate. The issue with this architecture however, is that upon power-up the PLL is in a manufacturer default frequency. As such a 25MHz crystal is used to clock automatic SPI and I2C transactions, to program the PLL and ADCs ready for data acquisition.

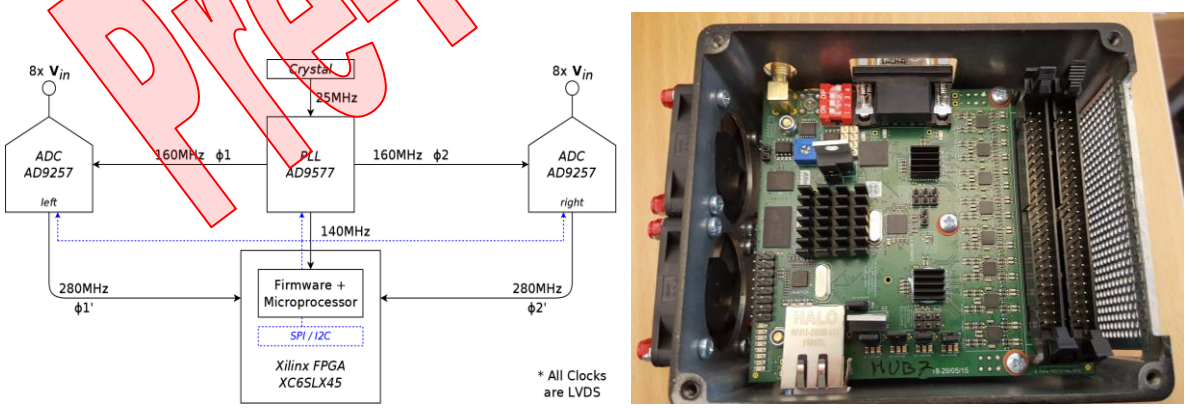


**Figure 4. (Left) Symmetric Low-Jitter, Low-Noise Clocking Architecture for the ADCs and FPGA Microprocessor, (Right) PCB detailing the FPGA, two Octal-Package ADCs and 16 Channel Analogue Inputs.**

## 3.4 Hub Design, Memory and Physical Interfaces

The Hub uses both design for test (DFT) and Design for Adaptability (DFAD) methodologies with the aims of providing easy system debugging and field programmability for use as a scientific instrument. DFAD is inherent in the use of FPGA technologies, allowing the firmware, embedded software and key

on-PCB circuits to be updated at the site of use. As such, the DAQ is not limited to the specifications of $CO_2$ gas sensing or TDLAS, but is a generalised DAQ structure.
To accommodate an embedded micro-processor, the Hub requires both high-speed volatile and low-speed non-volatile memories, in this case SDRAM and FLASH respectively. The FLASH memory is used as a large software instruction and data store during power-off, while the SDRAM acts as a working memory complementing the fast-access but finite Block-RAM memory of the FPGA. In order to interface to the out-of-test-cell data collection computer, the Hub incorporates a bi-directional 100BASE-TX (100Mb/s) Ethernet interface. This is used to transmit all acquired data and to receive run-time commands. To aid in development a UART-USB circuit is also used.

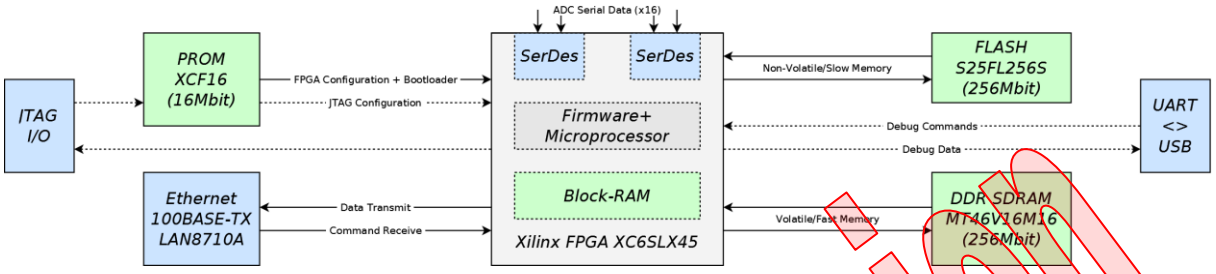


**Figure 4. FPGA System: Configuration via JTAG, PROM and Bootloader, Non-Volatile FLASH Memory, Volatile DDR SDRAM Memory, Ethernet and USB Interfaces and the 16 ADC SerDes Input Channels.**



## 3.5 DAQ Synchronisation Network and Strategy

Digital DAQs using TDLAS or DLIAs are inherently discretised into a) wavelength ramps, b) wavelength samples over that tuning range and c) discrete units of time representing the time constant of the DLIA. In Figure 5, the 100Hz wavelength tuning ramp is shown with the approx. 150-500kHz dither frequency (inset). The ramp is partitioned into software controllable start ('S'), acquire and finish ('F') periods to a) remove any laser settling and b) to prevent acquisition during laser 'fly back'.
The acquisition period is further partitioned into a number of wavelength samples ('I'), suitable for the spectrographic analysis used to obtain PCIs (Wilson et al 2014; Wright et al 2016), with each wavelength sample being made up of 'N' dither periods (time constant), and 'W' dither periods inter-sample waiting time (DLIA stop, sample and reset). While all parameters are controllable, the situation is restricted to integer values of the number of dither periods within the ramp. This ensures no fractions of a dither period remain unaccounted for, thus ensuring minimal phase walk.

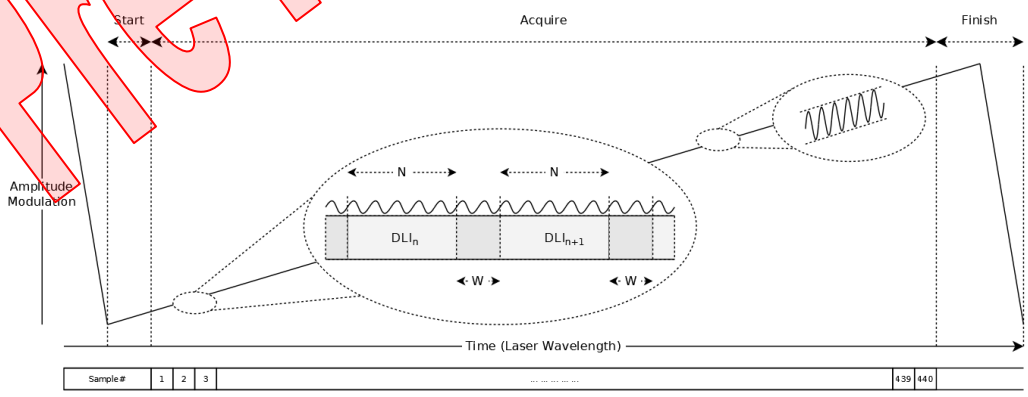


**Figure 5. TDLAS Data Acquisition Timing Methodology. The laser wavelength tuning ramp is shown with an inset zoom of the laser dither frequency, while DAQ sampling and windowing are also shown.**

The use of local DDS for the creation of the DLIA reference signal, gives a number of system level advantages. Firstly, the DDS is easily controllable in frequency and phase, secondly as it is multiplied with the input signal in the digital domain, the only appreciable reference noise sources are quantisation noise (14-bit), and sample clock jitter (synchronous with ADCs).

A third advantage comes from the manner in which the system is synchronised. The 12 Hub DAQ and the 16 channels per Hub require simultaneous sampling, start, acquire and finish times and assurance that all measurements have the same number of DLIA acquired and waiting periods. This synchronisation is not performed by distributing the laser dither as an analogue reference as distortion, jitter and noise would render a poor quality reference at the Hubs. Instead the synchronisation network supplies CMOS level (3.3V) digital signals in the form of a 100Hz square wave (proxy 'ramp') and a 150-500kHz square wave (proxy 'dither'). A nested finite state machine (FSM), then controls the DAQ progression in a controllable, discretised manner while supplying a clean locally generated reference.
The synchronisation network is therefore robust against electrical noise and routing delays are insignificant in comparison to the periods of the synchronisation signals. As the FSM is synchronous to a local Hub 100MHz system clock, jitter immunity in the synchronisation network is improved. This is the case as any change in time of arrival (skew) would also change the start time of the local reference. All channels of that Hub would therefore remain synchronous to each other, but would have a sampling point and recovered DLIA phase offset with relation to other Hubs on the ring. As this time offset would be an integer multiple of the local system clock, the resulting phase offsets would also be discretised and despite Gaussian jitter profiles, resynchronisation of this continuous time jitter would result in only a few offset possibilities. At the system level, this allows synchronisation cable length matching to be relaxed.

## 4 DATA ACQUISITION FIRMWARE/SOFTWARE DESIGN:

In this system we delineate the firmware design based upon signal processing tasks. The front-end interfaces to the real-world via the ADCs, performs the majority of signal processing and temporarily stores the data, while the back-end is defined as all transmission and control operations. The embedded C software runs on the microprocessor present on each of the 12 Hubs. This manages the DAQ at the local level providing unique addressed data packets, control over the operation of the Hub and the management of internal memory and data movement processes.

### 4.1 Hub Front-End Firmware

The Hub FPGA front-end firmware encompasses three main functions, a) ADC data grabbing using SerDes input channels (107.5Gb/s system total), b) data demodulation using an FPGA-based digital lock-in amplifier with local direct digital synthesis and c) both raw ADC data and demodulated DLIA data First-In First-Out (FIFO) memories for multiple synchronous channels (Figure 6).

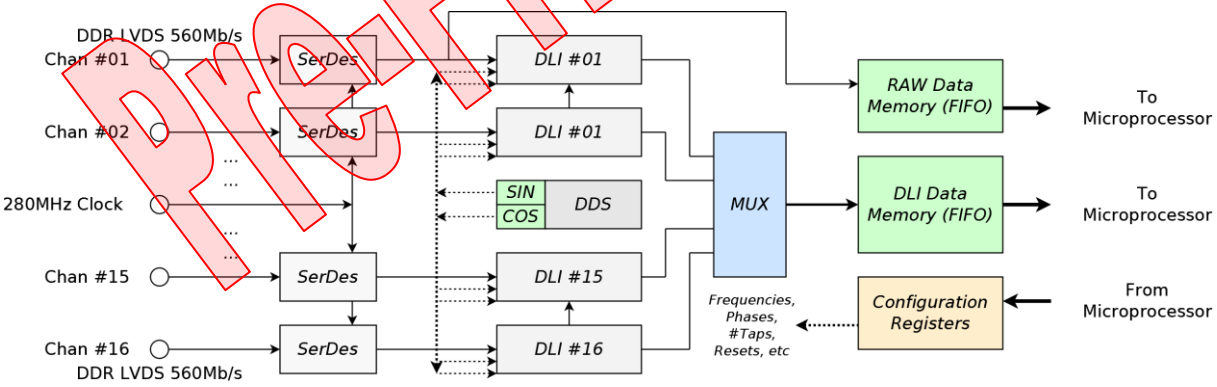


**Figure 6. Front-End Firmware Design showing ADC SerDes Inputs, DLIAs, DDSs and FIFO Memories.**

The FPGA-based DLI is of primary interest here as it allows an inherent decimation required to manage the data overhead, and allows real-time, configurable lock-in amplification of multiple parallel channels. To address the required reference frequencies first, these are generated locally by direct digital synthesis (DDS) at 40MS/s (14bit) (Figure 6). This allows frequency increments of 0.1Hz within the range 10kHz to 1MHz and removes the issues of analogue reference noise, distortion, and distribution. As mentioned in Section 3.5 the frequencies and harmonics for a given synchronisation system are restricted, however a combination of integer divisions of the ramp period and changes to timing parameters allows a wide frequency range to be used.
The frequencies and phases of both sine and cosine components are configurable and are locked to the modulation of the excitation laser. Each lock-in module utilises the dedicated 18bit multipliers

within the FPGA, this is followed by an accumulation acting as the low-pass and decimation of the DLIA (Chighine et al, 2015). A configurable number of DLIA samples (#Taps) is used a) allowing different DLIA time constants and b) a data decimation of SampleRate/#Taps. Due to the multiplication and addition operation, an increased data bit width is required, partially offsetting this data reduction. However here a bit width increase from 14bits to 32bits is offset by the large values of #Taps (typically 1000 to 2000). Due to the 1f, 2f, in-phase and quadrature DLIA outputs, the data decimation is further offset. A full system data output rate of 937.5 Mb/s (78.1 Mb/s/Hub) is expected in 192 channel mode and 615.2 Mb/s (51.2 Mb/s/Hub) in 126 channel $CO_2$ system mode (assuming #Taps=1000).

### 4.2 Hub Back-End Firmware

The back-end of the Hub firmware performs the majority of data acquisition tasks, in that it provides a) micro-processor Direct-Memory Access (DMA) to the signal storage FIFO buffers, b) the micro-processor itself (32-bit RISC Harvard architecture) with memory interfaces, c) control over the fabric logic and d) data transmission and reception of packaged data using the Ethernet network. Two critical issues arise in this section of the system. Firstly, as this PCB and micro-processor must interface to Commercial Off-The-Shelf (COTS) equipment – such as the data recording computer and the ring Gigabit Ethernet network – the Hubs must conform to all used standards of those COTS systems. Practically speaking, this forces the robust development of UDP or TCP/IP Ethernet protocols, and correct implementation of low-level control or memory architectures. Secondly, the remote nature of the Hubs from the human operator forces reliability concerns regarding data integrity, remote controls, the real-time performance of the micro-processor and of low-level functionality such as how to provide a suitable system or sub-system reset.

- The FIFOs and DMA must ensure data integrity, correct hierarchical data identification and pre-allocation and access to memory addresses accessible by the software heap (global variables) and stack (dynamically allocated finite scope variables) working memory.
- The micro-processor and its associated embedded C software must have both low memory utilisation and low total resource use on the finite resources of the FPGA. They must also be stable with respect to high-frequency hardware and software interrupts.
- The Ethernet transmission and reception system must correctly transfer packets using standard IP addresses, MAC addresses and Cyclic Redundancy Checks (CRCs). This impacts the final user PC as high level languages, require packet transmission up the entirety of the Open-Systems-Interconnection (OSI) or Internet-Protocol (IP) models.

Figure 7 shows the structure of the back-end firmware, where DMA is used via a custom Intellectual-Property Interface (IPIF) to move data from the RAW ADC or DLIA FIFOs into the micro-processor heap/stack memory. Once packaged this is transmitted via a Medium Access Controller (MAC) to the Ethernet Physical Layer (PHY). Control packets are also received, and if present in the MAC 'receive' buffer, are used to modify a) internal micro-processor registers or b) the configuration registers that interface to the fabric logic of the front-end firmware (Figure 6).

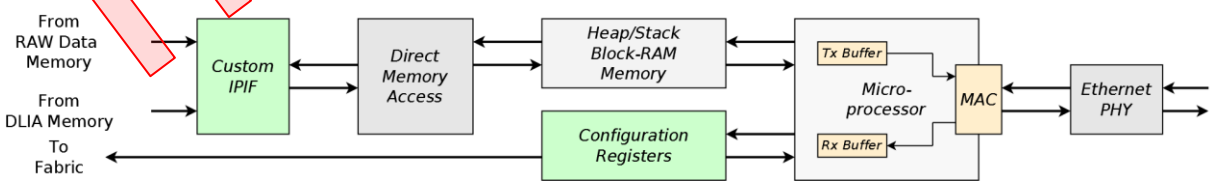


**Figure 7. Back-End Hub Firmware, detailing IPIF, DMA, Micro-processor, Heap/Stack Memory, MAC, Ethernet PHY and Control Configuration Registers. The RAW or DLIA data multiplexer in the IPIF is set using a configuration register.**

### 4.3 Data Integrity Improvements Through Data Interleaving

Packet loss in Ethernet networks is a function of a) traffic volume, b) the capacity of the network bottleneck, c) the Ethernet packet length and protocol and d) mechanical (connector movement) or electrical (noise) perturbation of the cabling. While cable shielding and locking connectors are used throughout, the UDP protocol is used within this first generation design. This protocol does not guarantee packet reception or packet order and does not support collision avoidance. Further, use of

Gigabit Ethernet PHYs was restricted on the Hubs due to MAC availability and reduction of DLIA data resolution (32bit to 16bit) was considered as a fall-back if packet loss became problematic.
As the spectrographic PCI recovery algorithm implements a least-squares fitting of the data with a calibrated analytic model (Bain et al, 2013), it is the shape of the DLIA demodulated gas absorption that is critical. With this in mind, and that a full ramp must be split into multiple Ethernet packets, packet loss would fundamentally remove all samples within a probabilistically varying region (Figure 8.a). If this occurs within the high gradient or critical absorption peak regions, a significant curve fitting error will result. To minimise the impact of this, a data interleaving approach is utilised, whereby sequential samples are directed to different packets with an interleaving ratio of 'M = {1, 2, 4, 8}' etc. Rather than a lost packet creating a discontinuity in the absorption line shape, a lost packet decreases the density of samples within that region, similar to variable bitrate sampling methods (Figure 8.b). In Figure 8.c, the curve fitting algorithm has been used with an ideal 2f input (+ Gaussian noise), this recovers PCI concentration with a particular error. A Monte Carlo method has been used with Poisson distributed packet loss, with the data points relating to the average concentration for 200 runs/point at a particular packet loss percentage. As packet loss becomes more severe, the error in curve fitting increases (Figure 8.d). However, data interleaving is able to retain the shape of the curve (Figure 8.b), allowing reduction of the fitting error for a particular level of packet loss.

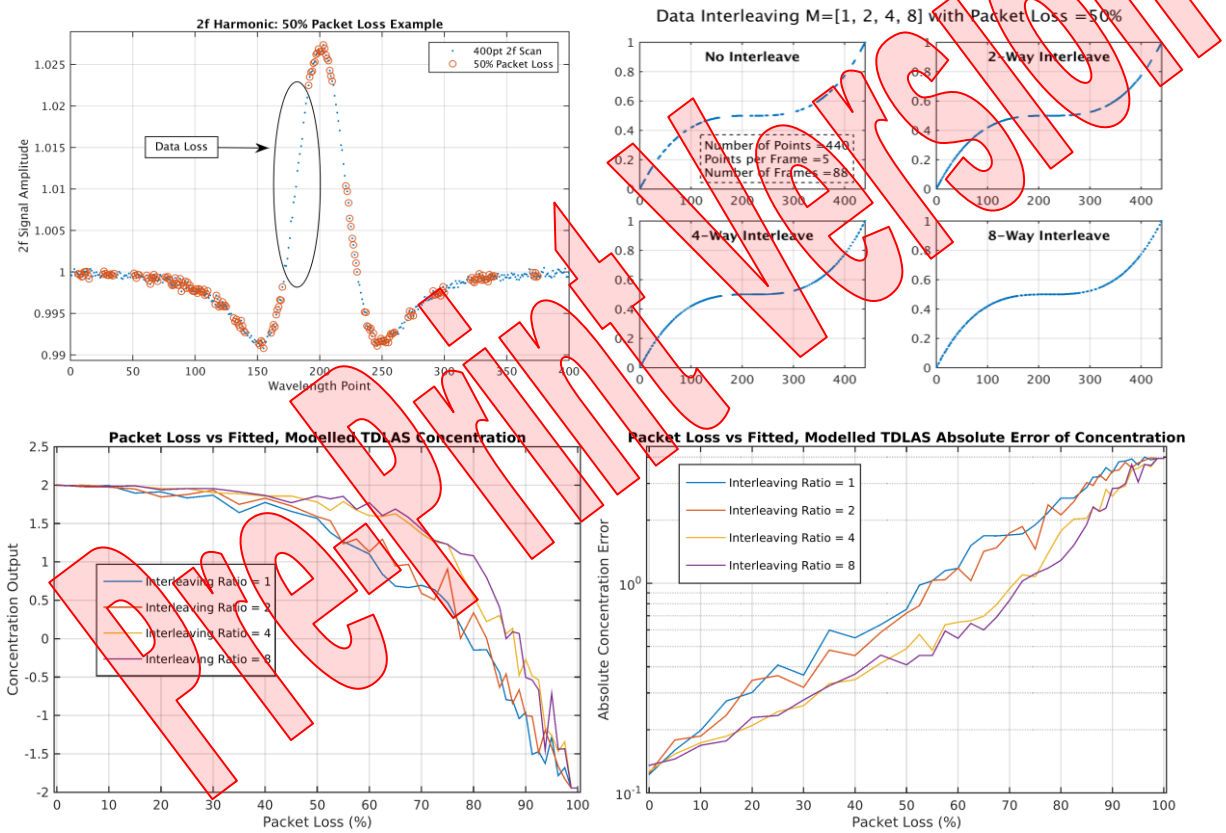


**Figure 8. a) Example of 2f Harmonic Data (blue), with 50% Packet Loss (red) and No Interleaving, b) Data Interleaving using M= {1, 2, 4, 8}, c) Decreasing PCI Gas Concentration, and d) Increasing Error with Increasing Packet Loss.**

## 4.4 Hub Embedded C Software

In order to create an instrument useful for scientific exploration, all critical parameters of the Hub can be modified from the software level. For example, the frequency and phase of the DDSs and DLIAs can be modified. This allows frequency sweeps a) measuring the noise profile of the engine and b) tailoring of the frequency to optimise the measurement SNR. The modification of the phase can be used to explore different components in the complex absorption measurement (Bain et al, 2013; Wilson et al, 2015).
As the DAQ Hub must be synchronous to the TDLAS modulation and to all other nodes, the synchronisation module (Figure 5) controls the software through the use of interrupts. However, as

interrupts can cause stability issues, a clear order of precedence with associated queues, buffers and known execution times are required.

- At the lowest, most infrequent level, the software polls the MAC Rx buffer upon each loop of the main() function while(true) loop. This ensures that if a command packet is received, it waits within that buffer until the processor is ready to execute it. This prevents command packets from interfering with the accessing or packaging of experimental data.
- The most critical interrupt, naturally has the highest priority. This is the data ready interrupt from the selected experimental data FIFO. If this FIFO is filled, the assertion of this flag interrupts any less important task, but only once the processor returns to the scope of the main() function. This allows command tasks to complete, preventing corrupted 'half finished' operations. Once the FIFO full interrupt is executed, it initiates a DMA transfer, via the custom IPIF, of FIFO data into a pre-allocated buffer within the heap memory of the processor. The processor then has full addressable access to this data allowing it to be passed into packet creation functions. Once a completed packet is passed to the MAC transmit buffer, the interrupt can return, as the MAC and PHY are able to operate in a parallel, pipelined manner.

# 5 INITIAL CHARACTERISATION/TEST RESULTS:

## 5.1 Hub Front-End Analogue Band-Pass / Anti-Alias Results

Testing of the Hub analogue front-end, including the high-pass and low-pass filters demonstrates 100% yield across all 192 populated channels. In Figure 9, the filter responses of a number of channels are presented indicating the correct a) 8Hz high-pass frequency, b) as designed, band-pass gain of approx. -0.7dB and c) approx. 3MHz anti-aliasing filter (Figure 3.). A separate test (solid black) was performed on Channel 5 of Hub 9 (H9C5 in Figure 9). This shows a flat gain response within the laser modulation range (150kHz to 500KHz), but some gain peaking (<1dB) prior to the low-pass roll off. While slight, this may introduce a frequency dependent offset between the recovered TDLAS laser dither 1st and 2nd harmonic terms. Deterministic, per channel offsets such as this can be calibrated for within the PCI recovery offline post processing. From a tomographic viewpoint, there is some gain non-uniformity of approx. 1.3dB within the frequency band of 100Hz to 1MHz. As this affects the recovered PCI, an indication of gain spread (at 100kHz) over all 192 channels is presented in Figure 9 inset. This shows a median of -0.59 dB, a standard deviation of 0.24 dB and a total range of 1.24dB. Due to the availability of fast multipliers within the FPGA, per channel weighting could be implemented in the future with a gain granularity of <0.1mV (assuming 2Vpp input).



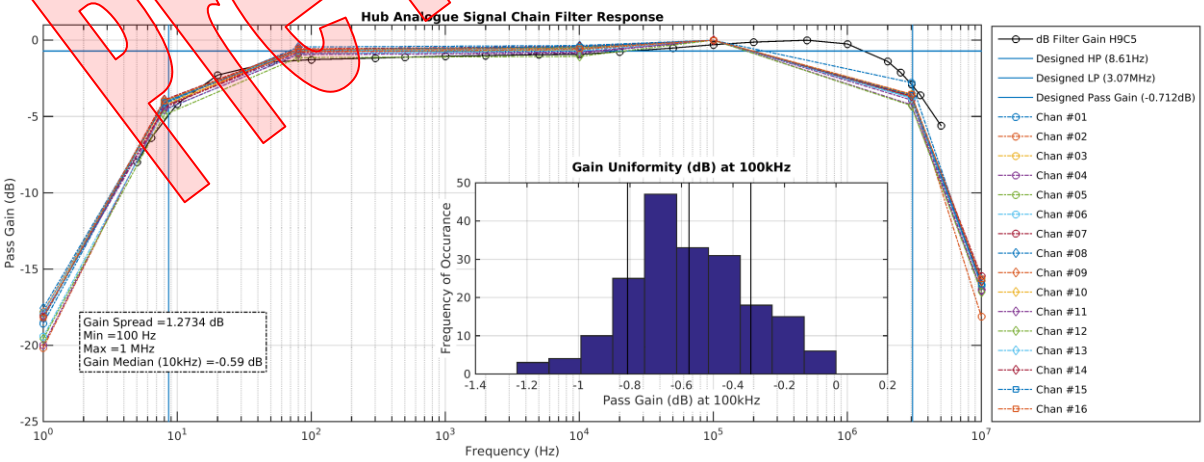


**Figure 9. Main: Hub signal chain pass-band for Hub #12 showing high- and low-pass roll off, and gain non-uniformity. Channel #5 of Hub #9 with extra frequency points, showing some gain peaking at the top of the pass band. Inset: Gain Uniformity (dB) of all 192 Channels at 100kHz. Mean = -0.57dB, Standard Deviation = 0.24dB, Range = 1.24dB**

# 6 CONCLUSIONS:

Robust measurement of jet-engine exhaust plume dynamics and gas species are critical for the development of novel engines, fuel mixtures and the overall reduction in pollutant emissions. At present few temporally and spatially resolved instrumentation solutions exist, and often utilise low-beam-count tomography or low frame rate direct imaging techniques. This paper seeks to increase tomographic beam count in a scalable manner and target specific chemical species of aviation relevance.

The system uses a hierarchical structure of photodiodes, pre-amplifiers, local digitisation hubs and Ethernet transmission. Further, FPGA-based digital lock-in amplification, local reference signal generation using direct digital synthesis and data interleaving are utilised to reduce reliance on rack-mounted equipment, the additive noise of traditional signal distribution and packet loss respectively.

Initial results have been presented for the DAQ structure analogue section, and all digital functionalities have now been developed. Per channel testing demonstrates 100% channel functional yield on the Hubs and approx. 98% pre-amplifier yield. It is expected that further characterisation, including that required for the spectrographic PCI recovery algorithm, is carried out in due course as the system is commissioned in the aero-engine test facility.



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